

**UTILITY
PATENT APPLICATION
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Attorney Docket No.	TESSERA 3.0-081 DIV CONT
First Inventor or Application Identifier	DiStefano, et al.
Title	Methods for Providing Void-Free Layers for
Express Mail Label No.	EL458418335US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages 29]
(preferred arrangement set forth below)
 - Descriptive title of the invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the invention
 - Brief Summary of the invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 9]
4. Oath or Declaration [Total Pages 1]
 - a. ☐ Newly executed (original or copy)
 - b. ☒ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

* NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.37), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.38)

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5. ☐ Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - a. ☐ Computer Readable Copy
 - b. ☐ Paper Copy (identical to computer copy)
 - c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (over sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement of Power of Attorney (when there is an assignee)
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
13. ☐ * Small Entity Statement filed in prior application, Status still proper and desired (PTO/SB/09-12)
14. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
15. ☐ Other: _____

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)of prior application No: 09 188,599Prior application information: Examiner K. PicardatGroup / Art Unit: 2822

For CONTINUATION or DIVISIONAL only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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METHODS FOR PROVIDING VOID-FREE LAYERS FOR SEMICONDUCTOR ASSEMBLIES

Cross-Reference to Related Applications

This is a continuation application of Application No. 09/188,599 filed
5 November 9, 1998, which is a divisional application of Application No. 08/610,610
filed March 7, 1996, now U.S. Patent No. 5,834,339.

Field of the Invention

The present invention relates to the field of semiconductor chip
packaging.

Background of the Invention

10 In the construction of semiconductor chip assemblies, it has been
found desirable to interpose encapsulating material between and/or around elements
of the semiconductor assemblies in an effort to reduce and/or redistribute the strain
and strain on the connections between the semiconductor chip and a supporting
15 circuitized substrate during operation of the chip, and to seal the elements against
corrosion.

Ball grid array ("BGA") packaged and chip scale packaged ("CSP")
semiconductor chips and flip chip attachment solutions are connected to external
circuitry through contacts on a surface of the chip. To save area on a supporting
20 substrate, such as a printed wiring board ("PWB"), these chips are directly
connected/soldered to the substrates and from there connected to external circuitry
on other parts of the substrate. The chip contacts are either disposed in regular grid
array patterns, substantially covering the face surface of the chip (commonly referred
to as an "area array") or in elongated rows extending parallel to and adjacent each
25 edge of the chip front surface. Many of the techniques for attachment run into
problems because of the thermal expansion mismatch between the material the chip
is composed of and the material the supporting circuitized substrate is made of, such
as a PWB. In other words, when the chip is in operation, the chip heats up and also

heats its supporting substrate thereby causing both the chip and the substrate to expand. When the heat is removed, the chip and substrate both contract. This heating and cooling process is referred to as "thermal cycling". Since the heat is being generated in the chip, the chip will heat up more quickly and will typically get
5 hotter than its supporting substrate. The materials comprising both the chip and the substrate have inherent expansion and contraction rates, referred to as their coefficients of thermal expansion ("CTE"), which causes them to expand and contract at different rates and in different degrees when subjected to the same thermal conditions. This thermal expansion mismatch between the chips and the
10 substrate places considerable mechanical stress and strain on the connections between the chip contacts and corresponding bond pads on the substrate.

BGA and CSP technology refers to a large range of semiconductor packages which use interconnection processes such as wirebonding, beam lead, tape automated bonding ("TAB") or the like as an intermediate connection step to
15 interconnect the chip contacts to the exposed package terminals. This results in a device which can be tested prior to mechanical attachment to the bond pads on supporting substrate. The BGA or CSP packaged chips are then typically interconnected with their supporting substrates using standard tin-lead solder connections. In most such packaged devices, the mechanical stress/strain due to
20 thermal cycling is almost completely placed on the solder connections between the chip and the substrate. However, solder was never intended to undergo such forces and commonly undergoes significant elastic solder deformation causing the solder to crack due to fatigue brought on by the thermal cycling. When the solder connections have smaller diameters, thermal cycling has an even more profound fatiguing affect
25 on the solder. This has driven efforts in the packaging art to modify the solder and other elements of the packages so that they may better withstand the thermal cycling forces.

As the features of semiconductor chip packages continue to be reduced in size, as in the case of CSPs, the number of chips packed into a given area will be greater and thus the heat dissipated by the each of these chips will have a greater effect on the thermal mismatch problem. Further, the solder cracking
5 problem is exacerbated when more than one semiconductor chip is mounted in a package, such as in a multichip module. As more chips are packaged together, more heat will be dissipated by each package which, in turn, means the interconnections between a package and its supporting substrate will encounter greater mechanical stress due to thermal cycling. Further, as more chips are
10 integrated into multichip modules, each package requires additional interconnections thereby increasing the overall rigidity of the connection between the module and its supporting substrate.

Certain designs have reduced solder connection fatigue by redistributing the thermal cycling stress into a portion of the chip package itself. An
15 example of such a design is shown in U.S. Patent Nos. 5,148,265 and 5,148,266, the disclosure of which is incorporated herein by reference. One disclosed embodiment of these patents shows the use of a chip carrier in combination with a compliant layer to reduce the CTE mismatch problems. Typically, the compliant layer includes an elastomeric layer which, in the finished package, is disposed
20 between the chip carrier and the face surface of the chip. The compliant layer provides resiliency to the individual terminals, allowing each terminal to move in relation to its electrically connected chip contact to accommodate CTE mismatch as necessary during testing, final assembly and thermal cycling of the device.

In some arrangements used heretofore, the compliant layer was
25 formed by stenciling a thermoset resin onto the chip carrier and then curing the resin. Next, additional resin was applied to the exposed surface of the cured layer, this additional resin was partially cured, and the resulting tacky adhesive surface was used to bond the elastomeric layer to the chip and chip carrier. Once attached, the

entire structure was heated and fully cured. Although this process is effective, further improvement would be desirable. The ambient gas can be occasionally entrapped when the chip carrier and die are affixed to the compliant layer. The entrapped gas can create voids and gas bubbles in the encapsulation of the surface of the die by the encapsulation material. These voids/bubbles allow moisture and other contamination to come into direct contact with the surface of the die. Accordingly, care must be taken to prevent such entrapment. This adds to the expense of the process.

In the flip-chip mounting technique, the contact bearing face surface of the chip opposes a bond pad bearing supporting substrate. Each contact on the device is joined by a solder connection to a corresponding bond pad on the supporting substrate, as by positioning solder balls on the substrate or device, juxtaposing the device with the substrate in the front-face-down orientation and momentarily reflowing the solder. The flip-chip technique yields a compact assembly, which occupies an area of the substrate no larger than the area of the chip itself. However, flip-chip assemblies suffer from significant problems when encountering thermal cycling stress because the sole thermal cycling stress bearing elements are the solder connections, as described above in relation to the BGA and CSP packages. In the case of flip chip devices, there is no package to redistribute the thermal cycling stress. Because of this, significant work has been done in the art to make the flip chip solder connections more reliable. However, to keep the chip's standoff from the substrate to a minimum, the solder connections have a typical diameter of between about five and eight thousandths of an inch ("mils"), too small to provide much real mechanical compliance. In an attempt to solve this problem, a curable liquid underfill is flowed between the chip and its attached substrate, enclosing the solder connections. The underfill is then cured into a rigid form which has a CTE that is closely matched to the solder material. The aim of the underfill is to reduce the stress caused by CTE mismatch by redistributing the stress more

uniformly over the entire surface of the chip, supporting substrate and solder balls.

Examples of the use of underfill materials may be found in U.S. Patent Nos.

5,120,678, 5,194,930, 5,203,076 and 5,249,101. All of these prior art solutions are

aimed at reducing the shear stress endured by the interconnections caused by

5 thermal cycling. However, each of these solutions also encounters significant problems such as insufficient compliancy, voids and process cost. Most significant among these costs is reducing the voiding problem which occurs when the underfill flows between the chip and the substrate and traps gas therebetween. If this gas is not removed, it will typically quickly expand during a heating cycle of the chip. The
10 force associated with the expanding gas can cause the solder connections to crack or otherwise become unreliable. Yet, presently, the underfill process involves a very costly and time-consuming process of allowing the underfill to flow very slowly between the chip and the substrate to try to avoid voids. After the underfill has flowed completely between the chip and the substrate, the assembly will then be
15 subjected to one or more vacuuming steps in a further attempt to remove any voids in the underfill material.

Despite these and other efforts in the art, still further improvements in interconnection technology would be desirable.

Summary of the Invention

20 The present invention provides a method of eliminating voids and gas bubbles within the encapsulation used in attaching and packaging microelectronic devices which solves the aforementioned problems in the art. The present invention further provides an effective method of filling cavities and channels during encapsulation of a plurality of semiconductor chips formed on a semiconductor
25 wafer.

In one embodiment, the method includes providing a substantially void and bubble free underfill for a semiconductor wafer having a plurality of flip chip assemblies. Typically, a flip chip device is electrically and mechanically attached to

a circuitized substrate, such as a PWB, by a plurality of conductive members, which are most typically a plurality of solder balls. These solder balls provide an electrical path from each chip contact to a respective bond pad on the substrate. The solder balls further provide a gap or stand-off between the wafer and hence each flip chip device and its substrate. This gap is then sealed on all sides of the flip chip device with a curable liquid encapsulant so that either a void (vacuum) or an area containing a first gas is thereby created. An isostatic or hydrostatic pressure is then applied to the semiconductor wafer assembly causing the encapsulant to flow into the gap and around the solder balls. An energy is applied to cure the encapsulant once the void/bubble has been completely removed thereby ensuring that new voids and/or bubbles do not re-occur between the flip chip device and the substrate. Typically, heat and/or ultra-violet radiation are used as the applied energy.

In another embodiment of the present invention, the method includes creating a substantially void/bubble free interposer layer between a semiconductor wafer having a plurality of microelectronic components and a sheet-like substrate. According to this method, an interposer layer is injected into a gap between each of the microelectronic components and the substrate such that any voids or gas bubbles are sealed within the gap. Isostatic or hydrostatic pressure is then applied to the entire semiconductor wafer assembly which causes the total volume for the voids/bubbles to be reduced to the point where they are substantially eliminated from the interposer layer. A further step of applying energy, such as heat, is employed to cure the interposer layer thereby ensuring that future void/bubble do not occur.

The injecting step may include providing a curable, liquid encapsulant at each edge of the gap between the microelectronic components and the substrate prior to the step of applying pressure, effectively sealing the space between the component and the substrate. When the pressure is then applied, it causes the sealed volume to be reduced thereby allowing the encapsulant to flow into the gap and form a substantially void/bubble free interposer layer.

A still further embodiment of the present invention includes a method of treating an interposer layer for a semiconductor wafer assembly to provide a substantially void/bubble free interposer layer. An interposer layer is first disposed between a semiconductor wafer having a plurality of semiconductor chips and a sheet-like substrate such that any voids within or at the boundaries of the interposer are sealed within the assembly. An isostatic or hydrostatic pressure is then applied to the assembly thereby reducing the volume of the voids/bubbles and substantially eliminating them from the interposer layer.

The foregoing and other objects and advantages of the present invention will be better understood from the following Detailed Description of a Preferred Embodiment, taken together with the attached Figures.

Brief Description of the Drawings

Figure 1A shows a top plan view of a flip chip device attached to a circuitized substrate having encapsulant sealing the edges therebetween, according to the present invention.

Figure 1B shows a fragmentary side view of the elements shown in Figure 1A, according to the present invention.

Figure 1C shows a bottom plan view of the elements shown in Figure 1A with the substrate removed from view, according to the present invention.

Figure 1D shows a bottom plan view of the elements shown in Figure 1A with the substrate removed from view and after full encapsulation, according to the present invention.

Figure 2A shows a top plan view of a semiconductor package assembly having an encapsulation sealing the edges of a gap between a sheet-like substrate and a semiconductor chip, according to the present invention.

Figure 2B shows a fragmentary side view of the elements shown in Figure 2A, according to the present invention.

Figure 2C shows a fragmentary side view of the elements shown in Figure 2A after full encapsulation, according to the present invention.

Figure 2D shows a perspective view of a plurality of chips attached to a substrate which is connected to a frame to support the substrate, according to the present invention.

Figure 2E shows a side view of a nozzle for depositing the encapsulant around the edges of the gap between the chips and the substrate in Figure 2D so as to seal the voids.

Figure 2F shows a perspective view of the a plurality of the frames show in Figure 2D are placed within a single carrier.

Figures 2G and 2H show cross sectional side views of two packaged devices, according to the present invention.

Figure 2I shows a face view of the chip package described in Figures 2G and 2H, according to the present invention.

Figure 2J shows a cross sectional view of a center bonded package as the void is being diffused into the encapsulation material, according to the present invention.

Figure 2K shows cut-away cross section A from Figure 2J depicting the collapsing of the void in response to isostatic pressure, according to the present invention.

Figure 2L shows a cut-away cross sectional view of a fan-in/fan-out embodiment, according to the present invention.

Figures 2M-1 through 2M-7 show the process of creating a void free layer by injection using the center bonded package shown in Figure 2J, according to the present invention.

Figures 2N-1 through 2N-7 show the process of creating a void free layer by injection using the center bonded package having a peelable compliant layer, according to the present invention.

Figure 3A shows a top plan view of a semiconductor package assembly having an interposer layer disposed between a sheet-like substrate and a semiconductor chip, according to the present invention.

Figures 3B and 3C show fragmentary side views of the elements shown in Figure 3A, according to the present invention.

Figure 3D shows a fragmentary side view of the elements shown in Figure 3A after the voids/bubbles have been removed, according to the present invention.

Figure 3E shows a fragmentary side view of the elements shown in Figure 3A after the package's leads have been encapsulated and the package is connected to a circuitized substrate, according to the present invention.

Figure 4A shows a perspective illustration of a semiconductor wafer having a plurality of chips for encapsulation in accordance with one embodiment of the present invention.

Figure 4B shows a perspective illustration of a semiconductor wafer having a plurality of chips for encapsulation in accordance with another embodiment of the present invention.

Detailed Description of a Preferred Embodiment

The present invention is directed toward the pressure injection of encapsulants into cavities and gaps in microelectronic structures and the simultaneous removal of voids and gas bubbles within encapsulants and adhesive/chip attach layers. As described below, the present inventive methods may be used as a method for underfilling attached flip chip devices, for injecting encapsulant and for removing voids and gas bubbles within encapsulants. As will be appreciated by one skilled in the art, each of the embodiments described below could and preferably would be performed on more than one assembly at a time to facilitate the mass production of finished parts.

I. FLIP CHIP UNDERFILL ENCAPSULATION

Figures 1A-D show a preferred method of providing a substantially gas bubble/void free underfill for a flip chip assembly, according to the present invention. Figure 1A shows top fragmentary view of a flip chip type assembly including a semiconductor chip 100, a supporting substrate 120 (such as a PWB), a plurality of electrical connections 110 interconnecting corresponding chip contacts (not shown) and bond pads (not shown) on the substrate 120. The solder connections both electrically and mechanically interconnect the chip contacts to the bond pads and, as best shown in Figure 1B, provide a "stand-off" or gap between the chip 100 and the substrate 120. Although many metals, conductive composites and alloys would be suitable to act as the electrical connections 110, the electrical connections 110 are typically comprised of an alloy of tin and lead, referred to generically in the semiconductor packaging industry as "solder balls". Figure 1C shows a bottom view of the assembly shown in Figure 1A with the substrate 120 removed from view.

As shown in Figures 1A-B and the side fragmentary view of Figure 1B, a curable, liquid encapsulant material 130 is deposited at each of the edges of the chip 100 so as to seal the gap between the chip 100 and the substrate 120 creating a sealed void or gas bubble 140 therebetween (depending on whether the surrounding environment has been evacuated prior to the sealing step). For the sake of simplicity, this void/bubble 140 will generically be referred to in this specification and in the claims as a "void". Typically, in flip chip embodiments, the encapsulant is comprised of a curable thermoset resin material. Since it is desired in a flip chip mounted device to have the encapsulant rigid after it is cured, an example of a suitable resin would include an epoxy resin, such as Hysol® epoxy sold by Dexter Corporation of Pittsburg, PA.

Isostatic pressure is then applied to the outside of the assembly. This step of applying more pressure on the assembly after the void 140 has been sealed will cause a pressure differential between the compressive, ambient gas applied to

the outside of the assembly and any first gas trapped within the void 140. The average diameter of the void 140 will thus be reduced allowing the encapsulant to begin encapsulating the outermost solder connections 110 on all four sides of the chip 100. This pressure differential further causes the encapsulant 130 to flow

5 between the chip and the substrate and around the connections. The amount of pressure required to collapse the void 140 depends on the type of encapsulant 130 used and on the desired time period to entirely collapse the void 140. Typically, if more pressure is used, less time is required to collapse the void 140. The amount of pressure applied may also depend on how the pressure is applied, i.e. all at once in

10 a virtual pressure "step" or gradually in progressively increasing pressure steps. While either pressure application method may be used, using one virtual pressure step increases the rate of collapse of the void 140. By way of example, the applied ambient gas pressure may be approximately between 10 and 1000 pounds per square inch ("psi") and will be applied for between thirty minutes to several hours;

15 although typically no harm will come to the assembly if it is allowed to remain within the pressurized environment beyond this specified time frame. Such pressure may be supplied by an autoclave device such as has been used in the aerospace industry; although the required size of an autoclave for the removal of voids within encapsulation is typically much smaller than required for the aerospace industry. An

20 example of a possible autoclave device is the Mini-bonder autoclave manufactured by United McGill of Westerville, Ohio.

Eventually, the trapped first gas in the void 140 will begin to reach an equilibrium state with the ambient pressure applied to the outside of the assembly, i.e. the pressure of the first gas (P_1) will be approximately the same as the ambient

25 pressure (P_2). At this time, the added pressure due to the surface tension (P_t) of the void 140 begins to play a more dominant role. As the void 140 gets smaller, the surface tension induced pressure acting on any first gas within the void 140 gets larger. At some point, during a second time period, the sum of the pressures within

the void 140 (P_1) will become greater than the ambient pressure (P_2) acting on the outside of the assembly. At or near this point, the first gas within the void 140 will slowly diffuse into the encapsulant 130. Since the gas within the void 140 is under higher pressure, during the second time period, than the ambient gas acting on the outside of the assembly, the rate of diffusion of the first gas into the encapsulant 130 will be greater than the rate of diffusion of the ambient gas into the encapsulant 130 causing the void 140 to get smaller still. As the diameter of the void 140 gets smaller and smaller, the pressure due to the surface tension (P_t) of the void 140 will progressively grow greater and greater, up until the point where the gas within the void is completely diffused within the encapsulant, as shown in Figure 1D, and the void implodes.

If the area around the flip chip device has been evacuated prior to the sealing step, there will of course be virtually no first gas within the void 140. This being the case, the combination of the ambient pressure (P_2) and the surface tension pressure (P_t) "push the encapsulant in to the void 140 while aided by a "pulling effect" created by the vacuum within the void 140 pulling the encapsulation into the void 140. Thus, an evacuation step prior to the sealing step will cause any voids 140 to collapse more quickly.

Typically, the next step includes applying energy to cure the encapsulant 130. The object of applying the curing energy is to fully cure (cross-link) the encapsulant 130 so that new voids will not reoccur such as may happen when the ambient gas pressure (P_2) is released quickly. The type of applied energy will depend on what encapsulant is used and how that particular encapsulant cures. Examples of possible sources of energy include heat, ultra-violet radiation, catalysis and combination thereof. When an epoxy, such as Hysol®, is used as the encapsulant, heat is typically applied as the curing energy. An appropriate temperature range will again depend on the type of encapsulant 130 used and the length of time desired to fully cure the encapsulant 130. A fully cured, thermoset

encapsulant 130 will maintain its structural integrity without allowing new voids to occur. It has also been found that the step of applying energy may occur after the ambient gas pressure (P_2) is removed from the assembly without the reoccurrence of voids 140 if the ambient gas pressure (P_2) is released slowly enough so as to allow
5 any dissolved gases within the encapsulant 130 to come to equilibrium with the surrounding ambient gas.

In a variation of this process, a first gas within the void 140 and an ambient gas may be comprised of different gases to facilitate the diffusion of the first gas into and through the encapsulant 130 at a greater rate than the rate of diffusion
10 of the ambient gas into the encapsulant. After the step of sealing the gap between the chip 100 and the substrate 120, the first gas surrounding the assembly may be evacuated and another ambient gas may take its place. In such an embodiment, the first gas contained within the void 140 may have smaller molecules than the ambient gas accelerates first gas' diffusion into the encapsulant 130. Choosing the correct
15 sealed first gas will necessarily entail choosing the correct ambient gas and vice-versa. Examples of sealed first gases include helium, hydrogen, H_2O vapor, etc. Examples of ambient gases when compared with the first gases listed above include argon, air, nitrogen, carbon dioxide and Krypton.

In a further variant of this process, hydrostatic pressure could be used
20 instead of the isostatic pressure discussed above to compress the voids/bubbles. Typically in such a process, inert fluids would be used to compress the voids/bubbles.

II. INJECTION OF AN ENCAPSULANT

As shown in Figures 2A-C, the methods described above in
25 connection with encapsulating flip chip device may also be used to inject a fluid encapsulant between a first intermediate substrate 225 and a chip 200 as well. One such embodiment where injection of encapsulation is described is in U.S. Patent Application Serial No. 08/365,699 filed December 12, 1994, which is hereby

incorporated by reference. In brief, as shown in part in Figures 2A-C, the '699 application describes a method and structure for disposing a plurality of compliant pads 250 which provide a stand off or gap between a first sheet-like support structure 225, and a contact bearing face surface of a semiconductor chip 200. The first substrate 225 may be rigid, semi-rigid or flexible. For added CTE compensation, preferably the first substrate 225 is a substantially inextensible dielectric film, such as polyimide having a thickness of between 0.5 mils and 3 mils.

As described above, the adjacent compliant pads 250 provide the structure for the gap between the chip 200 and the first substrate 225 and provide and define channels therebetween for the encapsulant 230 to eventually flow; however other alternatives could be used instead, such as cellular foam, loosely woven non-conductive strands, etc. It is only important that a gap be provided between the chip 200 and the first substrate 225 while holding the two items in a substantially coplanar relationship. The compliant pad embodiment will be described in this example. As described in the '669 application, the compliant pads 250 are typically deposited, as by stenciling, and cured so that the chip 200 and the first substrate 225 are attached to each other in a substantially coplanar relationship. A curable liquid encapsulant 230 may then be deposited completely around the perimeter of the gap between the chip 200 and the first substrate 225 so as to seal the pads 250 and create a sealed void (void/gas bubble) 240 out of the network of the channels therewithin, very much like the sealed assembly described in the flip chip embodiment above. Typically, a curable, compliant thermoset resin is used as an encapsulant, such as silicone and flexibilized epoxy. Alternately, thermoplastic materials may be used if they are specially formulated to undergo a phase change such that they go liquid under certain conditions and not under others, such as at a temperature which would be typically higher than the normal operating temperature of the resulting device.

An isostatic pressure is then applied to the assembly causing the encapsulant to flow between the chip 200 and the first substrate 225 and into the channels within the void 240. Again, the ambient gas pressure applied will depend on the encapsulant material selected and the amount of time desired for the process of removing the void 240; and further on whether the pressure is applied in a virtual step or is applied gradually. The typical applied ambient gas pressure here will be approximately between 10 and 450 pounds per square inch ("psi"), and preferably between about 30 and 200 psi, for a time period of between about thirty minutes and several hours (the time period also depends on the volume to be encapsulated). A virtual step of ambient gas pressure is preferred in order to increase the rapidity of the void removal.

As described above, the step of applying pressure on the assembly after the void 240 has been sealed will cause a pressure differential between the compressive, ambient gas applied to the outside of the assembly and any first gas trapped within the void 240. The average diameter of the void 240 will thus be reduced allowing the encapsulant to begin encapsulating the outermost compliant pads 250 on all four sides of the chip 200.

The pressure from the ambient gas combined with the pressure from the surface tension of the void 240 itself will cause the void to grow smaller. If there is a first gas trapped within the void, as the first gas pressure becomes greater than the pressure due to the ambient gas pressure, the first gas will begin to diffuse into the encapsulant 230. Since any first gas within the void 240 is under higher pressure, during the second time period, than the ambient gas acting on the outside of the assembly, the rate of diffusion of the first gas into the encapsulant will be greater than the rate of diffusion of the ambient gas into the encapsulant. As the diameter of the void 240 gets smaller and smaller, the pressure due to the surface tension of the void 240 will progressively grow greater and greater, up until the point

where the void 240 is completely removed from the encapsulant, as shown in Figure 2C.

As described in the last section, energy is typically applied to cure the encapsulant 230. The type of energy applied depends on the encapsulant 230 selected and under what conditions the selected encapsulant 230 cures. If a silicone is used as the encapsulant, the energy applied is typically heat. The amount of heat and the length of time the heat is applied is again dependent upon the selected encapsulant material and the volume of material that needs to be cured. As described above, the application of energy will typically occur prior to the termination of the step of applying pressure so that no new voids are allowed to develop in the encapsulant by the reduction of the ambient pressure. A fully cured, thermoset encapsulant 130 will maintain its structural integrity so that gas bubbles and voids do not reenter the encapsulant. The above mentioned variations and embodiments listed in the Flip Chip Underfill Encapsulation section, above, would also facilitate this injection process.

Thus, in the configuration shown in Figure 2C, the internal high stress zones in the chip package assembly are reduced by the substantial removal of the voids and bubbles in the cured compliant layer 270. This method of injection also works where the encapsulant is injected between a first substrate and a second substrate, such as in a fan-out chip package embodiment where at least some of the terminals 210 are disposed above a second support structure such as a thermal spreader or ring, as described more fully in the '669 application.

As described above and shown in Figures 2D-2G, the above injection methods are preferably performed on more than one assembly at a time to facilitate the mass production of finished parts. Figure 2D shows a perspective view of a plurality of chips 200 attached to a substrate 222, which includes the first substrate 225 and a sacrificial outer portion 227. An outer portion of the substrate 222 is also attached to a rigid or semi-rigid frame 280 to support the typically flexible substrate

222 such that it is stretched taut across the frame and further to better ensure the dimensional stability of the substrate. Since the combined thickness of the chips 200 and the substrate 222 is fairly thin, the thickness of the frame 280 is also typically thin so that a plurality of such assembled frames 221 may be placed in the same
5 pressure/temperature vessel after the encapsulant has been deposited, as described above.

Figure 2E shows a nozzle 235 for depositing the encapsulant 230 around the edges of the gap between the chips 200 and the first substrate 225 so as to seal the voids 240. A CAM/ALOT programmable dispensing machine
10 manufactured by Camelot Systems, Inc. in Haverhill, MA could be used to perform such a task. In this configuration, the encapsulant 230 is deposited from the chip side of the frame assembly 221. A layer of sheet-like material 229, such as a coverlay or solder mask material, is attached to the terminal 210 side of the substrate 222 so that the encapsulant is bounded and does not escape through the
15 bonding apertures 228 (Figure 2I) such that it could contaminate the terminals and thus impede any subsequent electrical connection of the terminals to the bond pads on the circuitized substrate 220. The frame 280 also acts as a barrier to provide a side boundary for the deposited encapsulant should the need arise. However, preferably, the encapsulant 230 has a thick enough consistency such that it
20 substantially maintains its shape through the surface tension of the material. Most preferably, the encapsulant 230 is deposited such that it does not flow onto the back surface (non-contact bearing surface) of the chip 200. This allows the back surface of the chip to subsequently be connected to a heat sink or thermal spreader without an insulative material impeding the dissipation of heat from the chip 200 during
25 thermal cycling.

After the gap has been sealed, the frame assembly 222 is placed within a pressure chamber, such as the aforementioned autoclave chamber, and an isostatic pressure is applied to collapse the voids and/or gas bubbles 240 thereby

causing the encapsulant to engulf the supports 250 and provide a substantially void free interposer layer, as described above. Preferably, a plurality of frames 280 are placed within a frame assembly carrier 285 so that the frames 280 may be more easily stacked together and placed within the pressure chamber. In the embodiment shown in Figure 2F, the frames are placed within the carrier 285 such that the opposite edges of the frames rest upon small shelves or projections 286 extending from the side walls of the carrier 285. In another examples, the frames 280 may simply be optimized such that a plurality of such frames 280 may be stacked one on top of the other such that the individual frames do not come into contact with the substrate 222 or chips 200 on an adjacent frame 280. Energy is then applied to cure the encapsulant, as described above.

The fully encapsulated semiconductor chip packages within the frame assemblies 221 are next separated (or "diced") from their respective frame/substrate into single packaged chips, such as that shown in Figure 2G, or the packaged chip may be diced into multi-chip modules. The dicing operation is typically performed by laser cutting, stamping or sawing (such as with a water saw). The component in Figure 2G has some benefits when compared with the embodiment depicted in Figure 2C. First, the first substrate 225 is extended to be the same size as the contact 270 bearing surface of the chip 200. This allows the cured encapsulant layer 230 (interposer layer) to have a substantially uniform thickness at every point between the chip 200 and the first substrate 225, even at the periphery of the package. This provides added support for the leads 260 during thermal cycling of the component as well as added physical and environmental protection for the metallurgy of the connection between the leads 260 and the contacts 270.

Figure 2H shows a side view of an alternate embodiment which is similar to the embodiment shown in Figure 2G. However, in Figure 2H, the first substrate 225 is juxtaposed with the contact 270 bearing surface of the chip, but is larger than the surface of the chip 200 such that it uniformly extends beyond the

perimeter of the chip 200. The interposer layer 230 correspondingly extends beyond the chip perimeter to form a bumper of encapsulant material 232. This structure may be created by dicing the packaged chips a short distance beyond the periphery of the chip 200 itself. The bumper 232 further protects the chip and the metallurgy of the connection of the leads 260 to the contacts 270.

Figure 2I shows a face surface view of the chip package described in Figures 2G and 2H. The bonding windows 228 allow the leads 260 to be detached from the sacrificial substrate 227 and be bonded to respective chip contacts 270.

Figure 2J shows a cross section view of a center bonded package as the void 240 is being diffused into the encapsulation material 230. The package in this Figure is similar to the package shown in Figures 2A and 2B except that in Figure 2J the die 200 is rectangular and the plurality of compliant pads 250 have been replaced by two compliant pads 250' which create a single center channel 240' therebetween instead of rows and columns of channels 240. Also, the leads 260' in Figure 2J are chip contacts which are located in a central portion of the contact bearing surface of the chip such that the leads 260' extend from either side of channel 240' and are bonded to the contacts in somewhat of an interleaving pattern, instead of being bonded to contacts which are peripherally positioned on the chip. The encapsulant 230 is again deposited at the edges of the gap created by the compliant pads 250' sealing void within channel 240'. Figure 2K shows cross section A from Figure 2J depicting the collapsing of the void 240' in response to isostatic pressure and any first gas contained within the void being diffused into the encapsulant, as described in the above embodiments. Figure 2L shows the same type of void 240'' collapse described above except that the compliant pads 250'' define a differently shaped void 240''. In this Figure, the compliant pads 250'' are located in the central portion of the chip 200 and beyond the periphery of the chip 200 (typically there is a support structure surrounding the chip to support the peripheral pads). This arrangement allows for a so called "fan-out" or "fan-in/fan-out"

semiconductor package embodiment in which the terminals 210 on the substrate 225 may be located in above the chip surface or beyond the chip's periphery or both, as described above.

Figures 2M-1 through 2M-7 graphically shows the above described
5 method (discussed in relation to Figures 2D through 2I) with respect to the center bonded embodiment of Figure 2J. In this embodiment, the chip 200 is attached to the compliant pads 250' attached to the tape 225. The tape has a bonding window so that the leads 260' may extend and typically detachably held in place thereacross. As shown in Figure 2M-2, the leads are detached from the substrate 225, guided
10 and bonded to respective chip contacts 270' using a bonding tool 231 which typically bonds the leads to the contacts using ultrasonic or thermosonic or thermo-compression means or some combination thereof, as shown. Figure 2M-3 shows a protective sheet-like layer 229, such as a coverlay or solder mask layer, is attached to the terminal 210 side of the substrate 222 so that the encapsulant may be
15 bounded and will not escape through the bonding apertures 228' so that it does not contaminate the terminals and impede any subsequent electrical connection of the terminals 210 to the bond pads on the circuitized substrate.

Figure 2M-4 shows a nozzle 235 depositing encapsulation material
230 around the chip 200 on the chip/compliant pad bearing surface of the substrate
20 222 so as to seal the gap/void 240' between the chip 200 and the substrate 225, as described in more detail above. It is evident from this that the protective layer 229 is performing the function of sealing any apertures in the substrate 225, such as the bonding aperture 228'. Figure 2M-5 shows the application of isostatic force and the resulting collapse of the void 240'. At this point, any gas which may be within the
25 void 240' diffuses into the encapsulation material 230 at a rate which is faster than the rate of gas diffusion from outside the sealed area causing the voids 240' to reduce in size and further causing the eventual removal of the voids 240', as shown in Figure 2M-6. Figure 2M-6 further shows the application of solderballs 211 to the

terminal sites 210. Figure 2M-7 shows a finished semiconductor package after it has been cut away (or “diced”) from the frame assembly, shown in Figure 2D, by laser cutting, stamping or sawing (such as with a water saw). In this particular embodiment, the package is diced such that a bumper 232 of encapsulation material is left along the side edges of the chip 200, similar to the embodiment shown in Figure 2H. In a variation, the package may be diced such that there is no bumper 232. In a further variation, a final step may be added in which a thermoset or thermoplastic resin sheet-like layer is vacuum laminated onto the back of the chip 200 and around each of the sides of the package to add further protection and durability to the package.

Figures 2N-1 through 2N-7 show a further variation on the processes and structures shown in Figure 2M-1 through 2M-7 in which a reworkable package structure is disclosed. In Figure 2N-1, a compliant layer 250''' is attached to the substrate 225 by means of a peelable tacky surface 251'''. This peelable compliant layer must be compliant enough to accommodate the CTE mismatch problems in thermal cycling of the finished device, yet have the ability to be removed (or peeled off) from the substrate 225 or allow the chip 200 to be removed after attachment without substantial residue on the substrate or chip. Examples of possible materials for the peelable compliant layer 230 include structures which have inherent releasable adhesive properties, such as pressure sensitive adhesives, and structures which may be “impregnated” so that they have such releasable adhesive properties, such as cured silicone pads impregnated with pressure sensitive adhesives or fully cured pads of tacky silicone gel, or fully cured compliant pad structures which have releasable adhesive on the major opposing surfaces.

As shown in Figure 2N-2 and described above, the chip 200 is then attached to the tacky surface 251''' and the leads are bonded. If there is a problem or defect with the package up to this point, the chip 200 may be removed and reused thereby providing a cost saving to chip manufacturers. Further, if the problem is with

the pad 230 and the lead bonding function has not occurred, the pad may be removed from the substrate 225 and a new pad 250''' may be used in its place.

Such a releasable package structure would encounter durability problems in use of the finished package due to the possibility of the pads 250'''/251''' peeling away from either the substrate 225 or the chip 200 or both unless, at some point before the package is shipped to a customer, the peelable nature of the pad is neutralized. Figure 2N-4 shows the encapsulant 230 being deposited on the substrate 222 at the periphery of the chip 200 so as to seal the area between the chip 200 and the substrate 225, as explained earlier. Isostatic pressure is placed on the assembly so as to reduce the volume of the void 240. As explained above, during this step, any first gas trapped within the void 240 diffuses into the encapsulant until the void 240 has been completely removed, as shown in Figure 2N-6. At this point, the encapsulant completely surrounds the peelable compliant pad 250''' thereby provided the needed means to bind the chip 200 to the substrate 225 prior to shipment to an end user, as shown in Figure 2N-7.

In a variation to this process, a pressure sealed membrane 231 may be applied or deposited in a sheet form atop the assembly, as shown in Figures 2N-5 and 2N-6, prior to the application of pressure thereby, in effect, laminating the membrane to the structure (back surface of the chip 200 and exposed surface of the encapsulant 230). Such a membrane 231 may be permanently sealed to the back of the chip 200 protecting the chip 200 and further binding the bumper portions 232 so that they do not de-laminate from the side edges of the chip 200 after the package has been diced, as shown in Figure 2N-7. Alternately, the membrane 231 may be removed from the back of the die leaving the back surface of the chip 200 bare to be subsequently attached to a cooling surface or heat sink.

In a still further variant of this process, hydrostatic pressure could be used instead of the isostatic pressure discussed above to compress the

voids/bubbles. Typically in such a process, inert fluids would be used to compress the voids/bubbles.

III. TREATING AN INTERPOSER LAYER

Figures 3A-E show a similar design to that shown in Figures 2A-C; however, in this embodiment, an interposer layer, such as a compliant pad 330, is disposed between the first substrate 325 and the semiconductor chip 300. The present invention provides a method of treating the pad 330 to provide a substantially void free layer. Typically, the compliant pad 330 is comprised of a curable thermoset resin, such as silicone, flexiblized epoxy, urethane elastomer or polyimide foam. In the embodiments shown in Figures 3A-E, the first substrate 325 is typically comprised of a substantially inextensible sheet-like material, such as polyimide, which may be substantially rigid, semi-rigid or flexible.

The pad 330 may be positioned and attached as a solid piece, as with adhesive on opposing sides thereof, or it may be stenciled or screened onto the face surface of the chip 300 or onto the opposing surface of the first substrate 325. Typically, it is stenciled onto the first substrate 325 prior to the leads 360 being detached from a sacrificial outer portion 327 of the first substrate and formed and bonded to respective chip contacts 370. The stenciled pad 330 is then at least partially cured. If a thicker compliant pad 330 is desired or if added adhesive properties are required a chip attach layer (not shown) may then be deposited on top of a typically fully cured pad 330, as by a stenciling step. The chip attach layer may be then be left either uncured or may be partially cured ("B-staged") prior to the attachment of the chip 300. Preferably, the chip is attached using a heated collet placement system so that the chip is relatively hot when it is pressed against the chip attach layer so as to minimize the number and size of any voids (or gas bubbles) 340/340'. Typically, these voids will occur at the boundary between the different materials in the assembly, e.g. first substrate/compliant pad, compliant pad/chip or even compliant pad/chip attach layer depending upon the materials chosen for those

two materials. Even using a hot chip placement system, gas bubbles or voids 340/340' are difficult to avoid in the uncured chip attach layer whether from the entrapment of gas when the chip is attached (Figure 3B) or when the pad 330 is stenciled (Figure 3C).

5 After the chip 300 has been attached and the voids 340/340' have been sealed within the package assembly, the assembly is placed under isostatic pressure for a given amount of time to remove the voids 340/340'. As in the embodiments described above, the step of applying an isostatic ambient gas to the outside of the assembly is used to create a pressure gradient between the lower
10 pressure first gas/vacuum within the voids 340/340' and the ambient gas pressure be applied to the outside of the assembly. This has the effect of compressing any first gas in the voids 340/340' thereby reducing the volume of the void and increasing the pressure therewith. If there is a sealed first gas within the voids 340/340', the pressure within the each void 340/340' is the sum of the pressure from the
15 compressed first gas and the pressure from the surface tension of the void. As the void volume decreases, the pressure from the surface tension of the void will increase dramatically. At some point during a second time period, the sum of the pressures within the void 340 will become greater than the ambient pressure acting on the outside of the assembly. Because of the greater pressure within the void in
20 relation to the pressure outside the assembly during second time period, the first gas within the void will begin to diffuse into the compliant pad/chip attach layer 330 faster than the ambient gas diffuses into the compliant pad/chip attach layer 330. The greater rate of diffusion of the first gas combined with the increased pressure of the first gas will cause the first gas to completely diffuse into the compliant pad/chip
25 attach layer 330 such that the bubble has been removed.

As described in the above sections, the pressure which is needed to remove the voids will depend on the materials used as the compliant pad and the chip attach layer and will also depend on the time allotted for their removal and the

total volume of the voids to be removed. An example of a suitable pressure/time range where both the compliant pad and the chip attach layers are comprised of silicone resin includes between about 10 and 1000 psi for anywhere over approximately one hour. The assembly may be kept under pressure for more than
5 the specified amount of time, without harm coming to it.

Any first gas sealed within the void 340 may be comprised of the same gas as the ambient gas; however, the first gas and the ambient gas may also be different in order to facilitate a greater rate of diffusion of the sealed first gas. After the step of sealing the first gas by attaching the chip to the compliant pad/chip
10 attach layer 330, the first gas present on the outside of the assembly may be evacuated and replaced with a different pressurized ambient gas. Desirably, the second ambient gas should have an inherent rate of diffusivity with respect to the chip attach layer material that is less than the rate of diffusivity of the first gas into the same chip attach material. If the chip attach material is a curable thermoset
15 resin material, suitable examples of possible first gases include: helium, hydrogen, H₂O vapor, methane and fluorinated hydrocarbons. Examples of suitable second ambient gases in such a situation include: argon, air, nitrogen, and carbon dioxide.

Typically, after the voids 340/340' have been removed from the compliant pad/chip attach layer 330, the assembly is heated in order to cure (or fully
20 cross link) the chip attach layer to ensure that the voids 340/340' do not return prior to the removal of the ambient gas pressure being applied the assembly. As described above, other types of energy may be used to cause the chip attach layer to cure depending upon what the material is comprised.

As shown in Figure 3D, after the voids 340/340' have been removed
25 and the compliant pad is cured, the leads 350 are typically detached from the sacrificial outer portion 327 and coupled to respective chip contacts 370. These leads are then encapsulated, as shown in Figure 3E, to protect them from corrosion and to support them during thermal cycling of the finished chip package assembly. If

voids are present in the lead encapsulant material, the voids may be removed by using the aforementioned methods. The encapsulation of the leads may also be performed using the same techniques described in the "back-side encapsulation" embodiment of Figures 2D-2H if the user desires to simultaneously produce a plurality of components.

In a further variant of this process, hydrostatic pressure could be used instead of the isostatic pressure discussed above to compress the voids/bubbles. Typically in such a process, inert fluids would be used to compress the voids/bubbles.

The method of the present invention has thus far been described with respect to individual semiconductor chips. However, it is contemplated that the method of encapsulation may be employed with a plurality of chips simultaneously provided on a semiconductor wafer. As illustrated in Figure 4A, chips 428 may be provided in the form of a semiconductor wafer 430 incorporating a plurality of such chips, all of the same design or of differing designs. Individual interposers 442 may be positioned on the individual chips 428 constituting wafer 430, and the interposers may be assembled to the chips as discussed above. In this operation, the contacts on each chip 428 are secured to the leads and terminals of each interposer. The encapsulation of the interposer 442 and chips 428 can be accomplished in accordance with the methods of the present invention as thus far described with respect to individual semiconductor chips. In addition, where an interposer 442 is omitted, encapsulation of the plurality of chips 428 on the semiconductor wafer can be achieved in accordance with the previously described process, for example, flip chip underfill encapsulation and injection of the encapsulant.

After the interposers 442 and chips 428 are encapsulated, the individual chips are separated from the wafer 430 and from one another, as by cutting the wafer using conventional wafer severing or "dicing" equipment commonly utilized to sever individual chips without interposers. This procedure yields a plurality

of encapsulated chips and interposer subassemblies, each of which may be secured to an individual substrate.

As illustrated in Figure 4B, a wafer 530 incorporating a plurality of interposers 542. Again, the contacts on each chip are secured to the terminals and leads of one individual interposer overlying the particular chip. The encapsulation of the chip and interposer may be accomplished in using any of the methods as thus far described. The wafer 530 and the sheet 535 are severed after this operation, and desirably after encapsulating, so as to provide individual subassemblies each including a chip and an interposer.

Having fully described several embodiments of the present invention, it will be apparent to those of ordinary skill in the art that numerous alternatives and equivalents exist which do not depart from the invention set forth above. It is therefore to be understood that the present invention is not to be limited by the foregoing description, but only by the appended claims.

What is claimed is:

1. A method of providing a substantially void free underfill for a semiconductor wafer having a plurality of semiconductor chips, comprising:
 - 5 electrically connecting a plurality of contact pads on a surface of a semiconductor wafer associated with a plurality of semiconductor chips to corresponding bond pads on a circuitized substrate such that the connections create a gap between the chips and the substrate;
 - 10 sealing the gap between the chips and the substrate with a fluid, curable encapsulant so that there is a void therebetween;
 - applying uniform pressure to the assembly causing the encapsulant to flow into the gap and around the connections, wherein the applied uniform pressure is between 10 and 1000 pounds per square inch; and
 - 15 applying energy to the assembly in order to cure the encapsulant.

ABSTRACT

A method for the removal of voids and gas bubbles within uncured or partially cured microelectronic component encapsulants and adhesive/chip attach layers. A sealed void or gas bubble within a gap between a microelectronic component and a supporting substrate is substantially eliminated through the application of a uniform pressure (isostatic or hydrostatic) and energy such that a substantially void/bubble free interposer layer is created.

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[illegible]

FIG. 1A

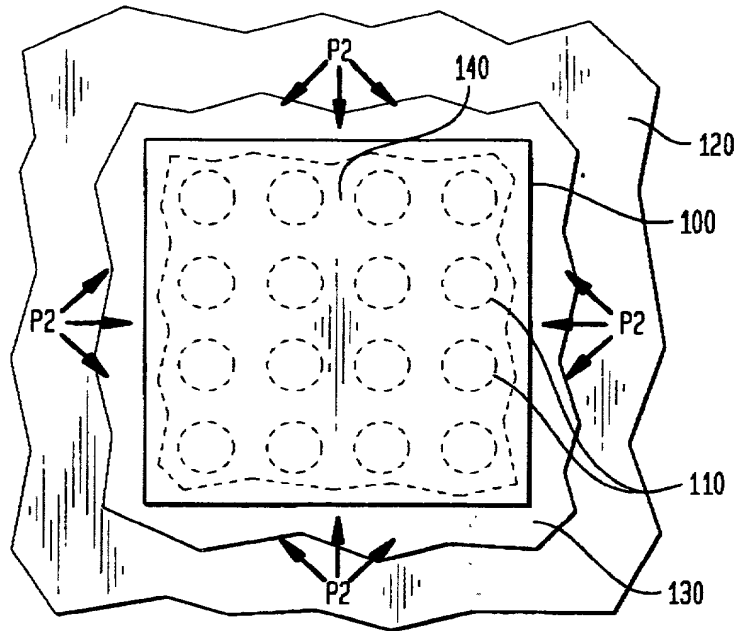


FIG. 1B

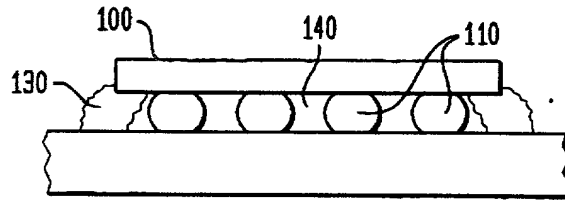


FIG. 1C

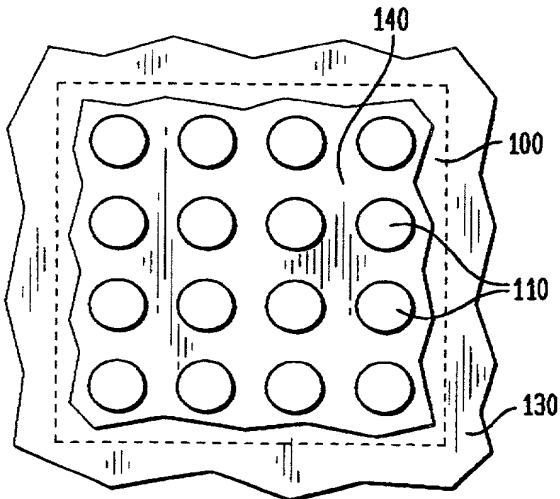


FIG. 1D

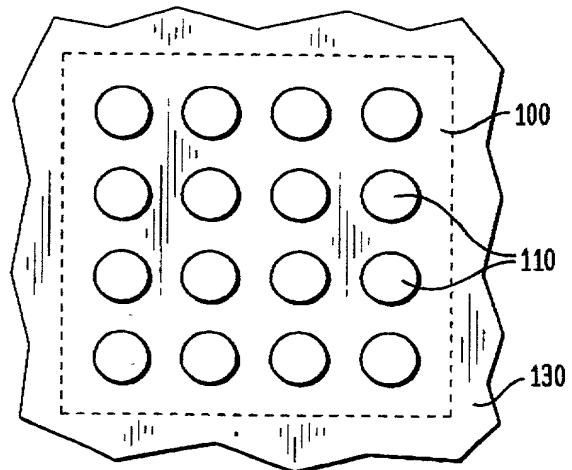


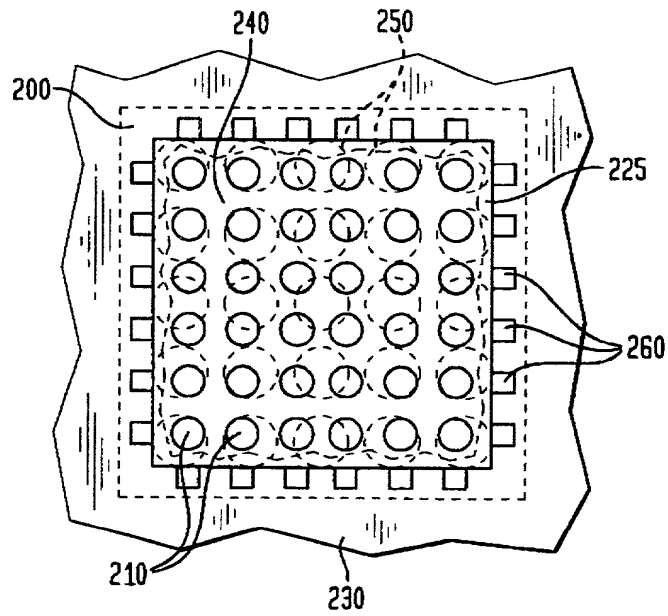
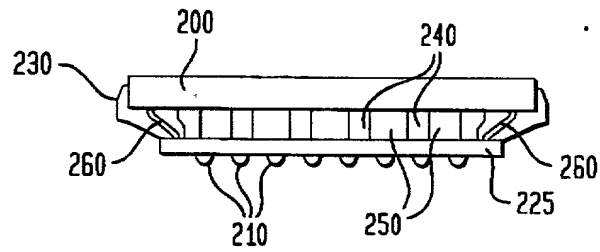
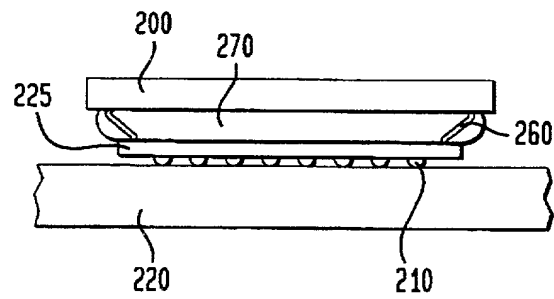
FIG. 2A**FIG. 2B****FIG. 2C**

FIG. 2D

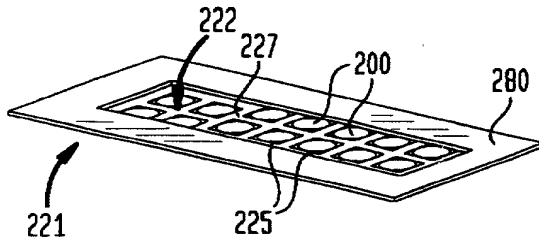


FIG. 2E

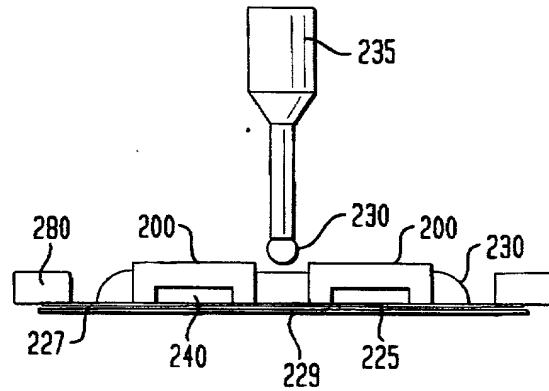


FIG. 2G

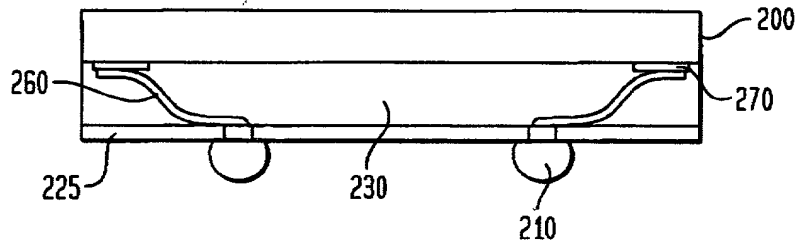


FIG. 2H

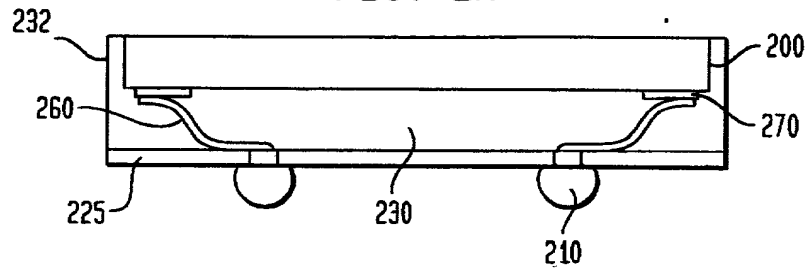


FIG. 2I

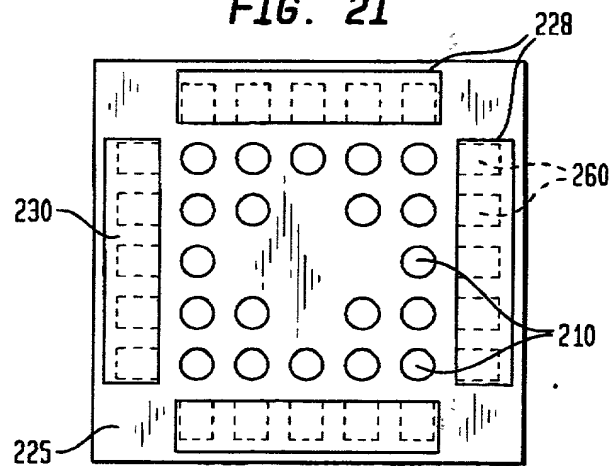


FIG. 2F

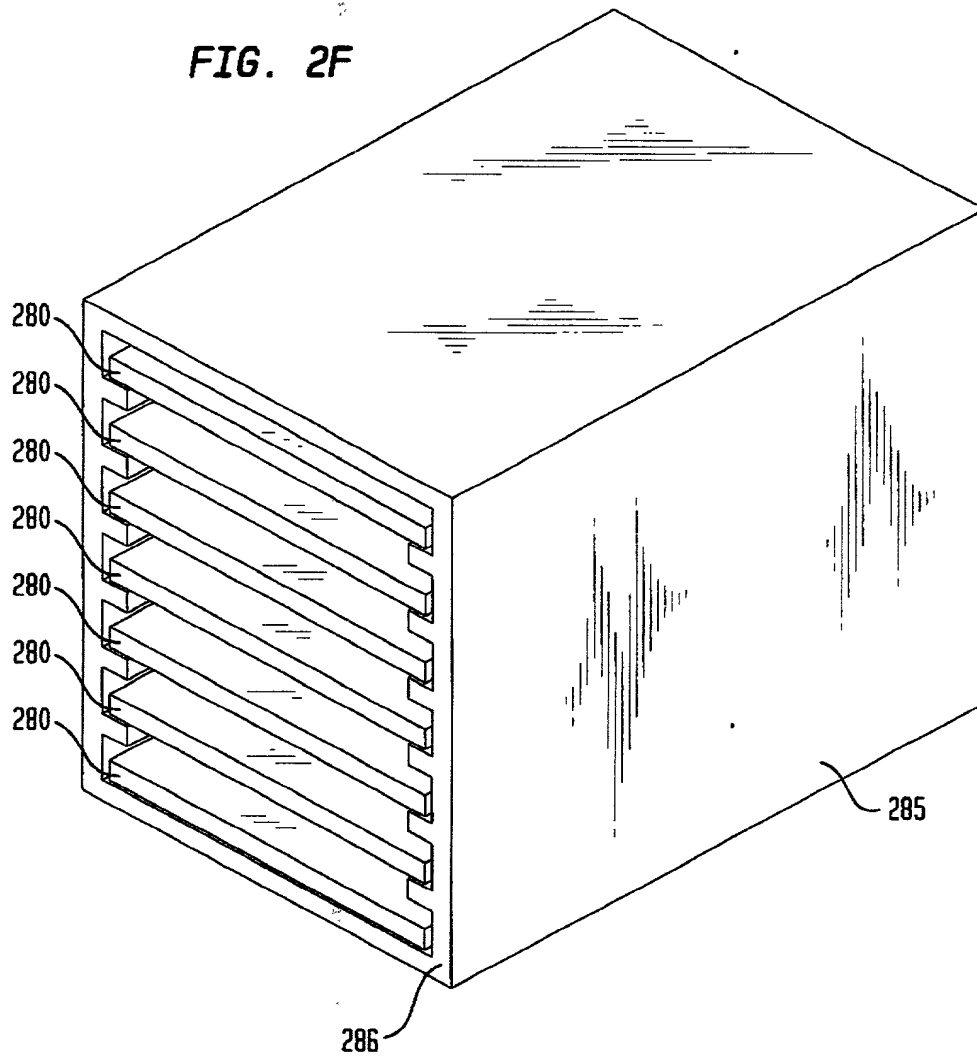


FIG. 2J

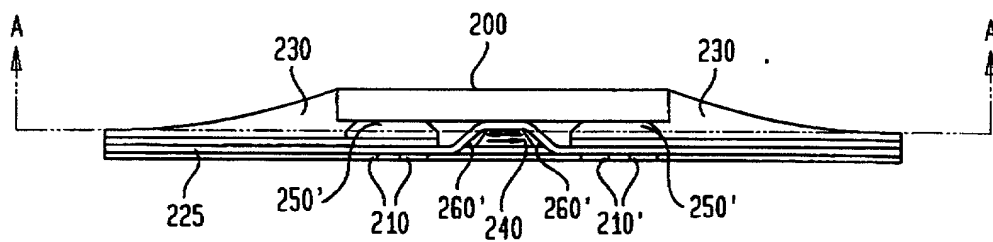


FIG. 2K

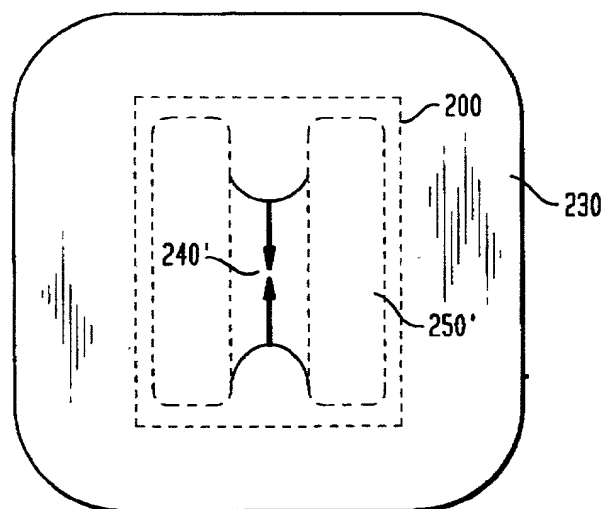


FIG. 2L

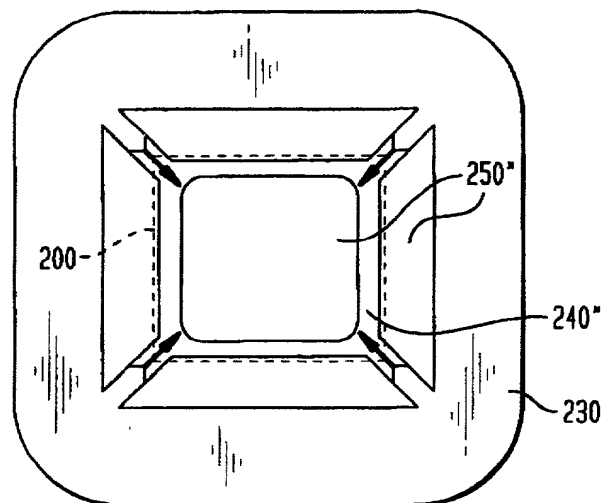


FIG. 2M-1

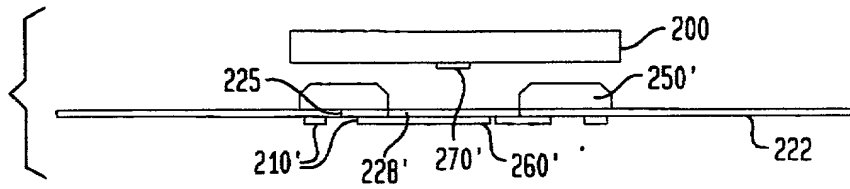


FIG. 2M-2

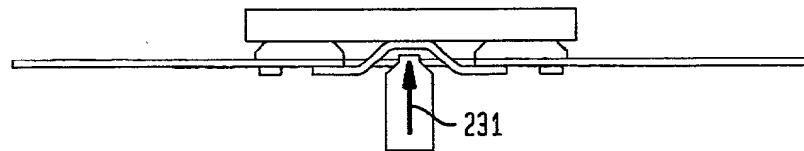


FIG. 2M-3

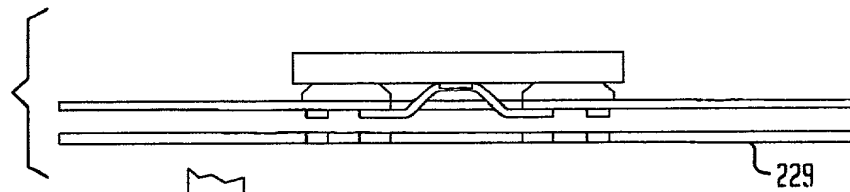


FIG. 2M-4

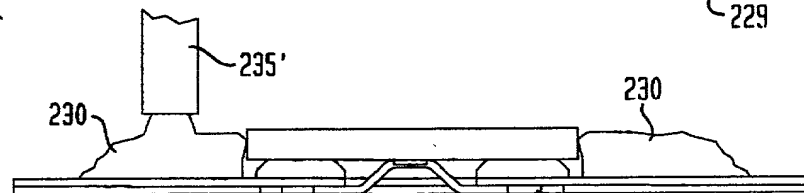


FIG. 2M-5

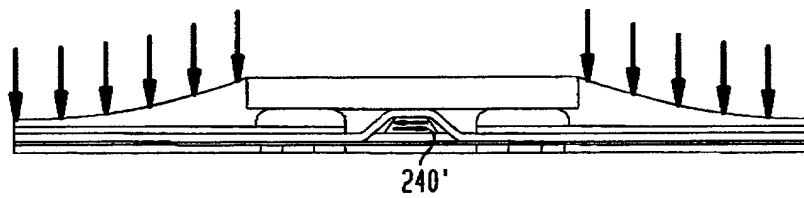


FIG. 2M-6

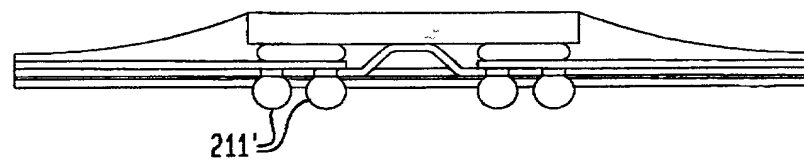


FIG. 2M-7



FIG. 2N-1

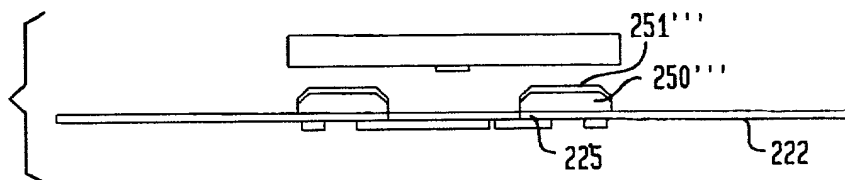


FIG. 2N-2

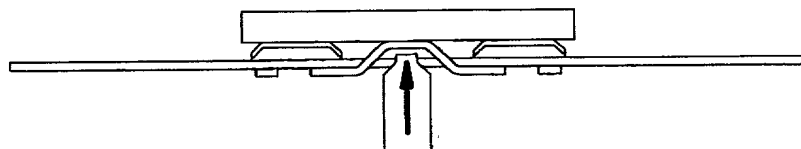


FIG. 2N-3

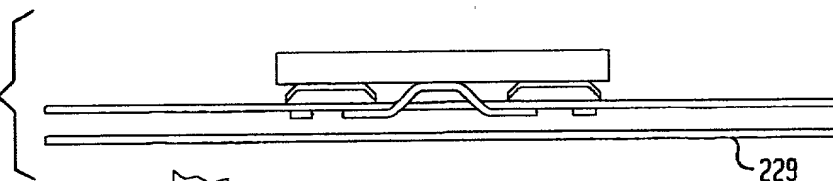


FIG. 2N-4

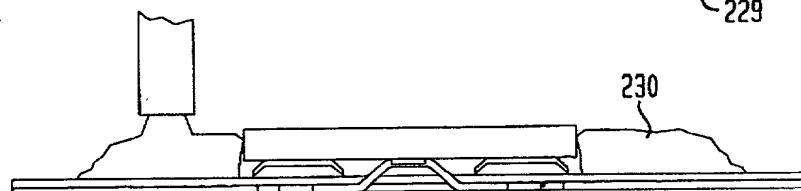


FIG. 2N-5

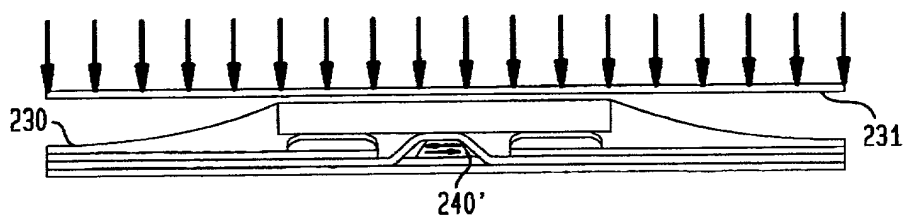


FIG. 2N-6

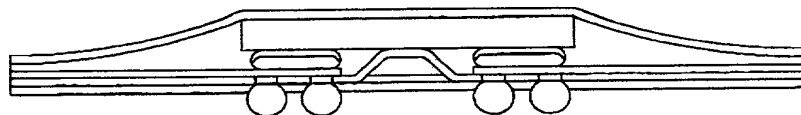


FIG. 2N-7

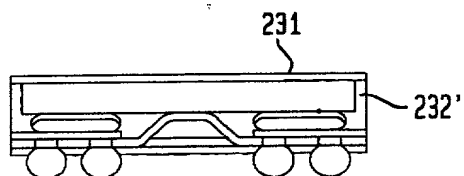


FIG. 3A

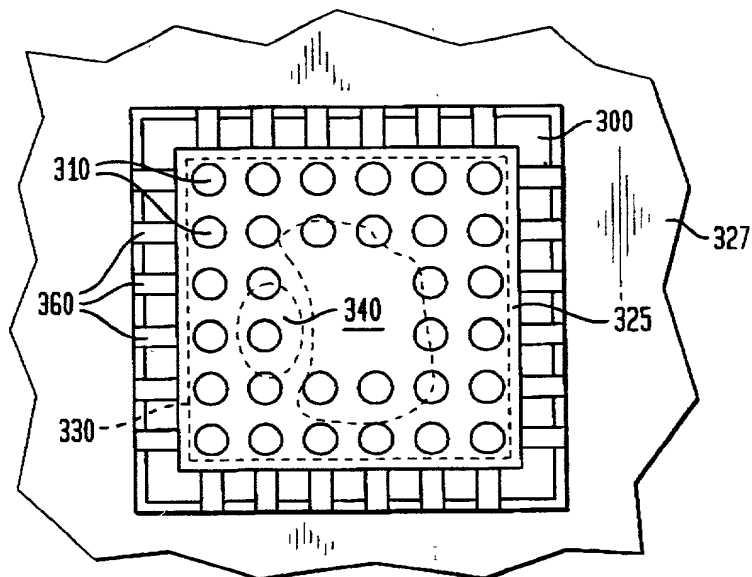


FIG. 3B

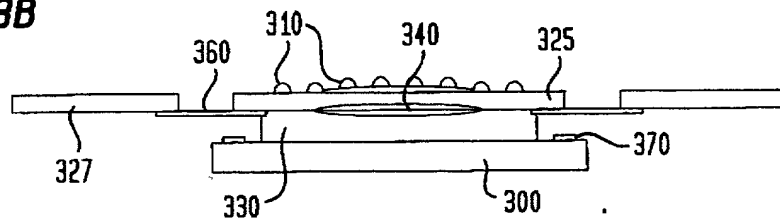


FIG. 3C

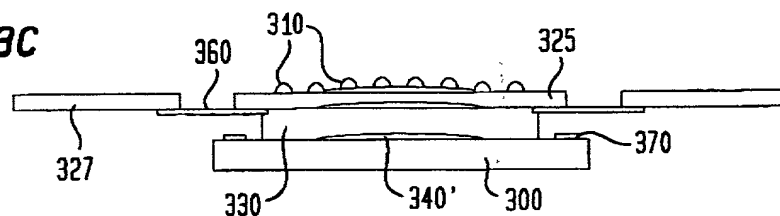


FIG. 3D

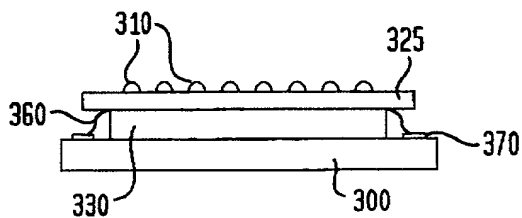


FIG. 3E

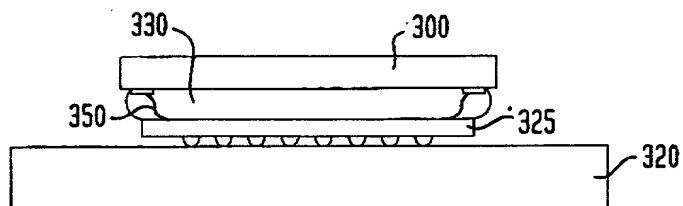


FIG. 4A

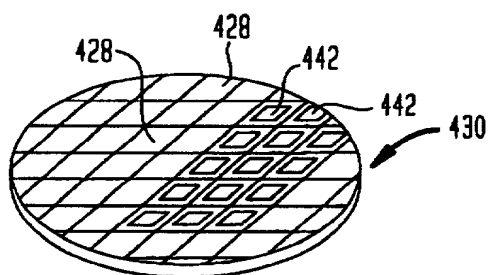
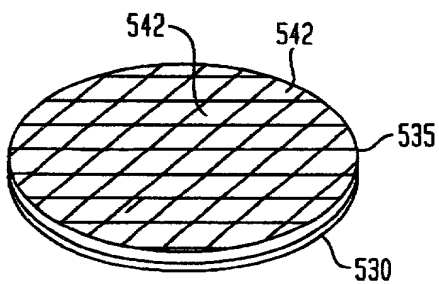


FIG. 4B



DECLARATION FOR PATENT APPLICATION

ATTORNEY'S DOCKET NO.: TESSERA 3.0-081

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHODS FOR PROVIDING VOID-FREE LAYERS FOR SEMICONDUCTOR ASSEMBLIES, the specification of which

☐ is attached hereto☒ was filed on March 7, 1996 as United States Application Number 08/610,610 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			YES <input type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>

LISTING OF FOREIGN APPLICATIONS CONTINUED ON PAGE 2 HEREOF ☐ YES ☒ NO

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Application Number:

Filing Date:

Application Number:

Filing Date:

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial Number:

Filing Date:

Status (patented, pending, abandoned):

Application Serial Number:

Filing Date:

Status (patented, pending, abandoned):

LISTING OF US APPLICATIONS CONTINUED ON PAGE 2 HEREOF: ☐ YES ☒ NO

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Lawrence I. Lerner, Reg. No. 19,516; Sidney David, Reg. No. 22,768; Joseph S. Littenberg, Reg. No. 20,832; Arnold H. Krumholz, Reg. No. 25,428; William L. Mentlik, Reg. No. 27,108; John R. Nelson, Reg. No. 28,573; Roy H. Wepner, Reg. No. 28,350; Stephen B. Goldman, Reg. No. 28,512; Paul H. Kochanski, Reg. No. 29,660; Marcus J. Millet, Reg. No. 28,241; Bruce H. Sales, Reg. No. 32,793; Daniel H. Bobbs, Reg. No. 18,694; Peter J. Butch III, Reg. No. 32,203; Keith E. Gilman, Reg. No. 32,137; Robert B. Cohen, Reg. No. 32,768; Arnold B. Dornien, Reg. No. 29,736; Michael H. Teeschner, Reg. No. 32,862; Jeffrey S. Dickey, Reg. No. 35,858; Gregory S. Gewirtz, Reg. No. 36,522; Jonathan A. David, Reg. No. 36,494; Shawn P. Foley, Reg. No. 33,071; Robert T. Canavan, Reg. No. 37,592; Christopher M. Pickett, Reg. No. 37,531.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor (given name, family name): THOMAS H. DISTEFANO

Inventor's signature

Date 8/21/96

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Post Office Address: 15363 ROBIN ANN LANE, MONTE SERENO, CALIFORNIA 95030

Full name of second joint inventor, if any (given name, family name) JOSEPH FJELSTAD

Second Inventor's signature

Date 8/21/96

Residence: SUNNYVALE, CALIFORNIA Citizenship: U.S.A.

Post Office Address: 1168 VASQUEZ #1, SUNNYVALE, CALIFORNIA 94086

☐ Additional inventors are being named on separately numbered sheets attached hereto.